METHOD AND CIRCUIT FOR HOT SWAP PROTECTION

FIELD OF THE INVENTION

[0001] This invention relates generally to protection circuitry, and more particularly to a method and system for inserting an un-powered circuit into a powered-on (hot) running system.

BACKGROUND OF THE INVENTION

[0002] As chip capacity continues to significantly increase, the use of programmable gate arrays (PGAs), particularly field programmable gate arrays (FPGAs), is quickly replacing the use of application specific integrated circuits (ASICs). An ASIC is a specialized chip that is designed for a particular application. Notably, an FPGA is a programmable logic device (PLD) that has an extremely high density of electronic gates as compared to an ASIC. This high gate density has contributed immensely to the popularity and flexibility of FPGAs. Furthermore, it has become a common industry practice to "Hot-swap" plug-in boards that contain integrated circuits such as FPGAs into powered-on systems.

[0003] Hot-swapping or hot insertion is a potentially dangerous method of inserting an un-powered board (containing integrated circuitry) into a power-on running system. Typically, concerns revolve around avoiding physical harm or permanent damage to the system or to the inserted board and avoiding data corruption or any transient system upsets.

[0004] Plug-in boards or printed circuit boards (PCB) typically need replacement in a system due to system failure, routine maintenance, or system upgrading. There are basically two ways of plugging in a PCB which contains a number of integrated circuit devices into a main system or a system backplane. One is to power down the whole system, plug in the board and then power up the system again. This

method fails to meet the reality and practicality of today's market demands requiring hot-swaps. The alternative is to plug in the boards or PCBs without powering down the system at the risk of damaging either the system or the boards being plugged in or both. There could be various reasons for the preference for hot swapping. For example, it may take too long for the system to be rebooted or the system performance could not be interrupted during repair work.

[0005] The problem that arises from hot swapping is the relatively long time it takes for the power to reach operating levels on the board due to the heavy capacitive load. Since the parts on the board are being connected to an active system, the input/output (I/O) pins of the integrated circuits on the board may see a logic level 1 (3.3v or 2.5v for example) long before the power is restored to the chip on the board. When this happens, due to the forward biasing of a pn junction diode at a pad of the board and due to the backward conduction of a pull-up driver at the pad, a high amount of current will flow through the package which may damage the system. Thus, a need exists to circumvent the problem described above when plugging in an integrated circuit microchip or a system board containing microchips into a powered-up system.

SUMMARY OF THE INVENTION

[0006] In a first aspect of the present invention, a hot swap protection circuit for an integrated circuit being plugged into a powered-up system comprises a first circuit for detecting a hot swap condition, a second circuit coupled to the first circuit for preventing a pn junction diode in a pull-up transistor from going into a forward bias condition, and a third circuit coupled to the first and second circuits for preventing the pull-up transistor from turning on during the hot swap condition.

[0007] In another aspect of the invention, a method of protecting a powered-up system during the insertion of an

integrated circuit comprises the steps of detecting a hot swap condition, preventing a forward bias condition in a pn junction diode of a pull-up transistor of the integrated circuit during the hot swap condition, and biasing the pull-up transistor coupled to a pad of the integrated circuit to remain turned off during the hot swap condition.

[0008] In yet another aspect of the present invention, a method of protecting a powered-up system during the insertion of a printed circuit board containing an integrated circuit, comprises the steps of detecting a hot swap condition, isolating an nwell of a pmos pull-up transistor from a power source of the powered-up system during the hot swap condition, and preventing the pmos pull-up transistor coupled to a pad of the printed circuit board from turning on during the hot swap condition.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. 1 is a circuit diagram of a hot swap detection circuit in accordance with the present invention.

[0010] FIG. 2 is a circuit diagram of a circuit that prevents a pn junction diode from going into forward bias conduction in accordance with the present invention.

[0011] FIG. 3 is a circuit diagram of a circuit that prevents a pull-up transistor connected to a pad from turning on in accordance with the present invention.

[0012] FIG. 4 is a system diagram including the circuits of FIGs. 1-3 in accordance with the present invention.

[0013] FIG. 5 is a cross-sectional view of a pmos pull-up transistor in accordance with the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

[0014] As previously mentioned, hot swap is referred to plugging in an integrated circuit device into a live or powered-up system. During hot swap, the input/output (IO) supply voltage (VCCO) can go up quite slowly due to the

capacitance on the VCCO line. But, the IO pins may see a logic level 1 (3.3v or 2.5v, etc.) immediately.

[0015] Preferably, a system in accordance with the present invention comprises a system to detect the hot swap condition. Preferably, this includes a system that detects both the beginning and the end of the hot swap condition. The system also comprises a circuit that prevents a p-n junction diode of a pull-up transistor from going into a forward bias condition. Finally, the system in accordance with the present invention also comprises a circuit for preventing the pull-up transistor coupled to a pad from turning on.

[0016] Referring to FIG. 1, a hot swap detector circuit 10 is shown in accordance with the present invention. A gate of the transistor 12 (P1) is connected to VCCO and the drain of transistor 12 is connected to a pad 16. If the voltage at the pad 12 goes a predetermined voltage level above VCCO, then the transistor 12 will begin to conduct and the node N0vcco will rise to the voltage level of the pad 16. This basically means that the hot swap is in progress or that a hot swap condition has been detected. When VCCO rise to within a predetermined voltage level of the pad 16 voltage level, transistor 12 will shut off and the transistor 14 (N0) which acts as a weak leaker will pull the N0vcco signal low indicating the end of the hot swap condition. It should be understood that in many instances the "predetermined voltage" in the examples described will actually be based on the threshold voltage of a PMOS transistor (Vthp). Thus, this predetermined voltage will usually be predetermined by process fabrication of the device involved.

[0017] Referring to FIG. 2 and FIG. 3, to prevent the NWELL of the pull-up transistor 32 (P4) from going into forward bias conduction, the NWELL needs to be disconnected from VCCO temporarily during the hot swap operation. The circuit 20 of FIG. 2 isolates the NWELL of pull-up transistor 32 from VCCO during the hot swap condition. The NWELL of

transistor 32 is connected to VCCO through the transistor 22 (P2). The gate of transistor 22 is connected to the N0vcco signal. As mentioned above, when a hot swap condition is detected, the signal N0vcco will go high (to the level of the voltage at the pad, which at this point would be at least a predetermined voltage higher than VCCO.) When N0vcco goes high, transistor 22 shuts off and the NWELL gets isolated from VCCO. Transistor 24 (P3) is biased similar to transistor 12 of FIG. 1. When the voltage at the pad 16 goes a predetermined voltage above VCCO, transistor 12 begins to conduct and will charge the NWELL to the level of the voltage at the pad 16 hence preventing the NWELL's pn junction diode from going into a forward bias condition. When VCCO rises to a predetermined level of the voltage at the pad 16, transistor 24 shuts off, the signal N0vcco goes low which turns on transistor 22 and biases the NWELL to VCCO again.

[0018] Referring to FIG. 3, one of the pad's discharge paths during hot swap is the pmos pull-up driver or transistor 32. The circuit 30 cuts off the flow of current through transistor 32 during the hot swap condition. When a hot swap is detected, meaning the signal at the pad 16 is a predetermined voltage higher than VCCO, then the N0vcco signal goes high and forces the output of the NOR gate 37 low. Transistor 38 (P7) turns on and pulls up the gate of transistor 32 high to the pad voltage and in effect turns the transistor 32 off. Transistor 38 turns transistor 32 off by directly supplying voltage of the pad 16 to transistor 32's gate. Transistor 34 pre-drives the signal to turn transistor 32 off. If the voltage at node G1 goes up, then transistor 34 will be on because the gate of transistor 34 is still low. During the charge up of a node G1 shown in FIG. 3, transistor 36 is turned off by signal N0vcco allowing the charge to remain on node G1 as long as necessary to keep transistor 32 off. The transistor 33 (N1) preferably serves to pull down the IO circuit. Transistor 35 (N2) preferably serves as a normal NMOS pull down to activate transistor 32

during normal operation. After Novcco goes low, transistor 36 (P6) will turn on and normal operation is restored.

[0019] Referring to FIG. 4, circuits 10, 20 and 30 are combined to form circuit 40 as shown. Once circuit 10 detects the hot swap, the NWELL and node G1 are charged to the pad voltage and there will not be any current flowing through either the pn junction of transistor 32 or the transistor 32 itself (the pmos pull-up transistor) connected to the pad 16.

[0020] Referring to FIG. 5, The NWELL of the pmos pull-up driver transistor 34(P4 in Fig.3 and Fig.4) is usually tied to VCCO. The drain of the transistor 34 is connected to the pad 16. The cross section 50 of this configuration is shown in Fig. 5. When the drain (pad) is higher than the NWELL (VCCO), then the pn junction diode 52 at the pad side of the transistor (the drain) will turn on and a lot of current will flow through the transistor. The second current path is the PMOS pull up transistor 32(P4 in Fig. 3) itself. When the pad voltage is higher than the VCCO and also higher than the voltage at the gate of the transistor 32, the transistor 32 turns on and conducts backward (current flows from pad to VCCO). The present invention takes care of both of these situations by disconnecting the NWELL from the VCCO and by turning the transistor 32 off during hot swap.

[0021] In light of the foregoing description of the invention, it should be recognized that the present invention can be realized in hardware, software, or a combination of hardware and software. A method and circuit for hot swap protection according to the present invention can be realized in a centralized fashion in one computer system, or in a distributed fashion where different elements are spread across several interconnected computer systems. Any kind of computer system, or other apparatus adapted for carrying out the methods described herein, is suited. A typical combination of hardware and software could be a general-purpose computer system with a computer program that, when

being loaded and executed, controls the computer system such that it carries out the methods described herein.

[0022] The present invention can also be embedded in a computer program product, which comprises all the features enabling the implementation of the methods described herein, and which, when loaded in a computer system, is able to carry out these methods. Computer program or application in the present context means any expression, in any language, code or notation, of a set of instructions intended to cause a system having an information processing capability to perform a particular function either directly or after either or both of the following a) conversion to another language, code or notation; b) reproduction in a different material form.

[0023] Additionally, the description above is intended by way of example only and is not intended to limit the present invention in any way, except as set forth in the following claims.